OPEN ACCESS

University of BRISTOL

Gamlath, C., Arabi, E., & Morris, K. A. (2018). A design technique for concurrent multiband tunable loads from 0.4–6GHz with independent Q tuning. In *2017 IEEE Asia Pacific Microwave Conference (APMC 2017): Proceedings of a meeting held 13-16 November 2017, Kuala Lumpur, Malaysia.* (pp. 980-983). Institute of Electrical and Electronics Engineers (IEEE). https://doi.org/10.1109/APMC.2017.8251615

Peer reviewed version

License (if available):
Other

Link to published version (if available):
10.1109/APMC.2017.8251615

Link to publication record in Explore Bristol Research
PDF-document

This is the accepted author manuscript (AAM). The final published version (version of record) is available online via IEEE at https://doi.org/10.1109/APMC.2017.8251615 . Please refer to any applicable terms of use of the publisher.

University of Bristol - Explore Bristol Research
General rights

This document is made available in accordance with publisher policies. Please cite only the published version using the reference above. Full terms of use are available:
http://www.bristol.ac.uk/red/research-policy/pure/user-guides/ebr-terms/

A Design Technique for Concurrent Multiband Tunable Loads from 0.4-6GHz with Independent Q Tuning

Chris Gamlath, Eyad Arabi, Kevin A. Morris, Mark Beach
Computer Systems and Networks Group
University of Bristol
Bristol, BS8 1TR, U.K.
chris.gamlath@bristol.ac.uk, eyad.arabi@bristol.ac.uk, kevin.morris@bristol.ac.uk, m.a.beach@bristol.ac.uk

***Abstract*—This paper presents a preliminary attempt at designing a concurrent multiband tunable load. Each band is independently tunable and the centre frequency of each band can be placed anywhere from 400MHz to 6GHz. This is done through the use of high frequency impedance inverters which enable each band to be tuned independently. The design has been implemented in a low cost 0.25μm BiCMOS process using 1μm HBTs operating at 1.2mA from a +/-2.2V supply. The circuit is targeted at 5G wideband applications requiring narrow band filtering where the bandwidth also needs some degree of tunability. The results show that high Q factors of over 100 can be achieved and that the individual bands show independent tunability. Although the circuit is demonstrated for three bands it is easily extendible to a higher number of bands.**

***Index Terms*—5G, BiCMOS, LNA, Tunable, Multiband, Active Inductor**

I. Introduction

The recent proposal of carrier aggregation standards for 5G LTE systems indicates the requirement for multiband concurrent operation of receivers from 400MHz to 6GHz with up to 5 concurrent bands. On the hardware side this creates a significant filtering challenge for receivers and particularly for the low noise amplifier (LNA). The challenge is mainly with interference rejection filtering schemes required to operate in multiple bands with each band tunable across the entire frequency range. While it is possible to duplicate single band receivers in parallel, this solution is unattractive both in terms of cost and power consumption. A more attractive solution is sought which employs a single main amplifier with only parts of the circuit or subcircuits having to be duplicated. Ideally these subcircuits would occupy a low die area and power consumption thus providing multiband filtering without paying much of the penalty. The most common technique for achieving this is the integration of the filtering into the gain of the low noise amplifier through the use of tunable loads. Reference [1] shows one example where the use of high-Q tunable loads at the output of the LNA circuit enables a frequency selective gain function. This presents high gain to the wanted signal while presenting a much lower gain to the interferer signals. Other examples can be found in [2] and [3]. A further use of high-Q tunable loads is at the RF input where the blocker frequencies are heavily mismatched in comparison to the wanted band as shown in [4]. When extending these ideas to the multiband case it is only the tunable loads that need to be duplicated.

This paper looks at one technique for extending single band loads to multiband loads where each load can be tuned independently. A previous paper [5] has shown the design of a single band active inductor (AI) high Q load with a tunable centre frequency and Q factor. This load will be developed into a triple band architecture in this paper. Tunable loads based on AI resonant circuits have been shown to provide very high Q factors in excess of 100 [6], [7] and forms an attractive alternative to frequency translational loads [1]–[3]. The AI implementation also has a lower power consumption due to the low transconductance of the metal oxide semiconductor field effect transistors (MOSFETs) used. This provides a significant advantage over the larger power consumption of frequency translation architectures [8] which makes use of mixers in the filtering path. The low power of AI based architectures allows duplication to multiple bands with lesser impact on the total power consumption. The major drawback however is the increase in noise voltage when the Q factor is increased [7]. However several implementations of AI circuits for LNA applications that make use of the noise cancelling technique have been successfully demonstrated in CMOS to overcome this problem [9]–[11].

The architecture described in this paper also makes use of the recently available high Q tunable capacitors based on micro-electro-mechanical systems (MEMS) and Barium Strontium Titanate (BST). The primary advantage of these technologies is the wide tuning range and higher power handling capabilities compared with on-chip varactors. These also have the advantage of having very small form factors thus saving printed circuit board (PCB) area. The performance of these components is constantly improving at radio frequency

This project is funded by EPSRC (Engineering and Physical Sciences Research Council, U.K.) Grant No. EP/M01360X/1.

(RF) frequencies [12] and are already finding use in antenna tuning circuits [13]. The combination of these technologies with complementary metal oxide semiconductor (CMOS) processes is currently an active area of research [14].

Section II discusses the basis for operation of the proposed circuit. Results from a 0.25μm bipolar and complementary metal oxide semiconductor (BiCMOS) process are shown in section III followed by concluding remarks.

II. Theory and Design

A block diagram of the proposed architecture is shown in Fig. 1. The impedance input presents a frequency variable impedance that can be connected to the amplifier. The nature of this connection depends on the particular amplifier architecture. In the case of Fig. 1 the triple band impedance shows dips in impedance at the carrier frequencies of the three wanted bands. However these can be changed to peaks depending on the requirement of the amplifier with the addition of another impedance inverter before the multiband impedance input point shown in Fig. 1.

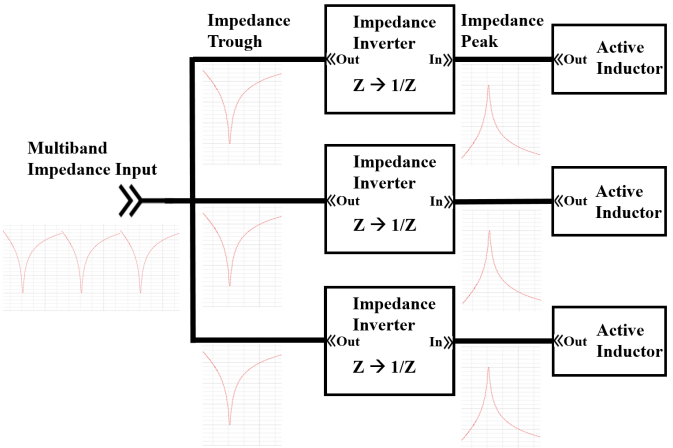

Fig. 1. Block diagram of multiband system showing impedance profile at each point along the chain.

A. Active Inductor Block

The simplified circuit schematic of the AI block without bias details is shown in Fig. 2. The maximum stable Q factor at 6GHz has been shown to be just above 600. The fundamental equation (1) governing the resonant frequency and Q factor is shown below where C_3 is the external capacitor and C_1, C_2 are on-chip varactors.

$$Z_{in}(s) \approx \frac{\frac{s}{C_1} + \frac{g_3}{C_1 C_3}}{s^2 + s\left(\frac{g_1}{C_1} + \frac{g_3}{C_3} + \frac{g_1 g_3 C_2}{C_1 C_3 G} - \omega^2 \frac{C_2}{G}\right) + \frac{g_{m1} g_{m2} g_{m3}}{G C_1 C_3}} \quad (1)$$

g_1 to g_3 are the output conductances of the individual transconductors as shown in Fig.2. g_{m1} to g_{m3} are the transconductances and C_1 to C_3 are the capacitor values. The factor G represents the value of g_{m1} + g_{m2} - g_2.

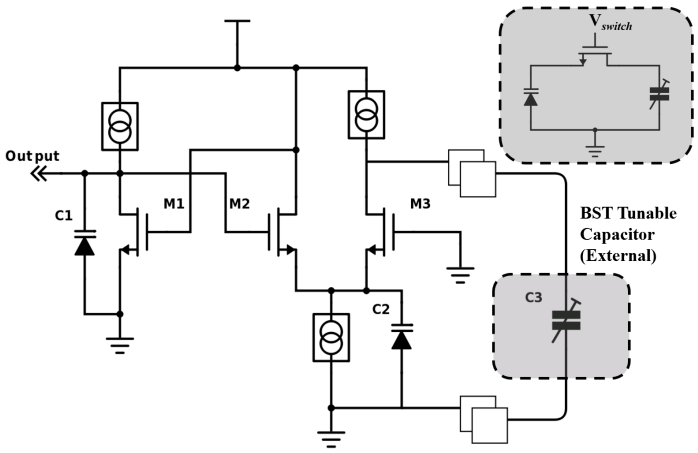

Fig. 2. Schematic of active inductor block without bias details. Inset shows implementation of C_3 as the combination of an on chip varactor, a MOSFET switch and an external MEMS/BST tunable capacitor.

The capacitance C_3 of Fig. 2 is implemented as an external BST capacitor. These capacitors are commercially available in small form factors with a 2pF 5:1 tuning ratio capacitor available in less than 0.15mm^2 die area. Capacitor C_3 is implemented as an on chip varactor in series with an on chip MOSFET switch and an external BST capacitor. The switch is turned on for frequencies below 3GHz allowing the off chip capacitor to dominate the capacitance. In the off state the capacitance of the bond pads along with the on chip varactor and parasitic capacitances enable frequencies close to 6GHz to be reached. The combined capacitor C_3 along with capacitor C_1 sets the centre frequency while capacitor C_2 sets the Q factor. For example a centre frequency of 5.6GHz can be reached using C_1=250fF, C_2=100fF, C_3=500fF. In this state the analysed results show a Q factor of 106 with an input impedance level of around 25KΩ at the resonant frequency of 5.6GHz. The linearity of the circuit is limited by the linearity of the two transconductors formed by M1 and the M2, M3 pair. A detailed description of circuit operation along with details of the AI block can be found in [5].

B. Impedence Inverter Block

The individual tunable AI blocks are combined with the use of impedance inverters to form a multiband tunable load. The output of the impedance inverter (Fig. 3) shows the reciprocal of the impedance presented at the input. The combined response is the reciprocal of the sum of reciprocal impedances and has the same form of an admittance. This can be converted back to an impedance by adding an extra impedance inverter at the combined impedance input point.

Each impedance inverter stage is formed using two CCII- (second generation negative current conveyors) stages. The block diagram is shown in Fig. 3. The CCII has simultaneous

voltage follower and current follower properties. The voltage at terminal X is followed by terminal Y and the current in terminal X is conveyed to terminal Z. The details of how the connection of the two CCII- forms an impedance inverter is shown in [15]. The circuit diagram for each CCII- is shown in Fig. 4. This is very similar to the architecture shown in [15] except that the output stage is cascoded using Q2. This allows operation of the circuit to be extended close to 6GHz. All HBT transistors had an emitter length of 1μm, an emitter width of 420nm, a y-multiplier of 1 and an x-multiplier of 2. The value of R1 can be from 500Ω to 1KΩ and sets the value of minimum output impedance achievable. The results are discussed in the next section.

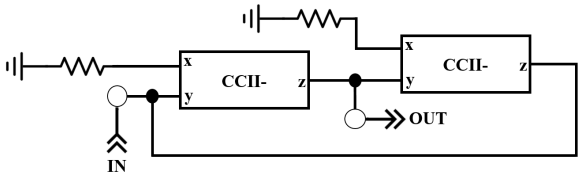

Fig. 3. Block diagram of impedance inverter block.

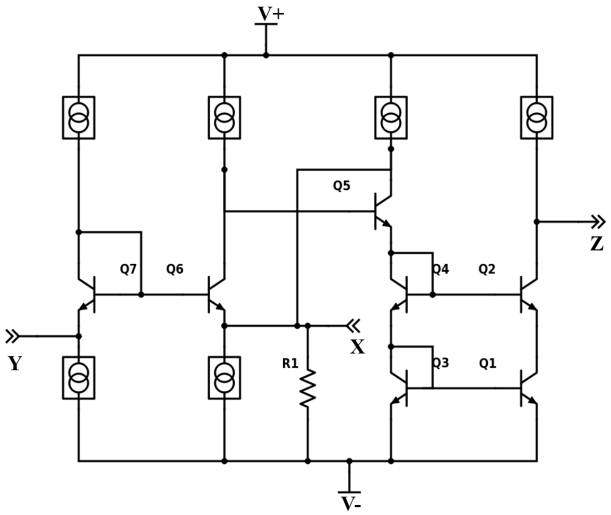

Fig. 4. Circuit diagram of each current conveyor block (CCII-).

III. Results

The proposed architecture was implemented in a 0.25μm BiCMOS process using 1μm HBT transistors. The simulation results presented here have used the Cadence Virtuoso IC design toolkit and contains highly accurate foundry verified models for the process technology under simulation. All simulations were performed using Cadence Spectre with BSIM3 models for the transistors including post-layout parasitics and the simulations with typical corner are presented here. The capacitors of each active inductor (AI) unit have been tuned such that the impedance peaks appear at 420MHz, 2.9GHz and 5.6GHz. Each AI can be tuned across the entire band from 400MHz up to near 6GHz. The maximum frequency achievable in this circuit is 5.6GHz and is limited by the parasitic capacitances and other layout parasitics of the transistors used in the AI circuit.

Fig. 5 shows the effect of tuning AI stages 1 and 3 to different frequencies while the capacitor values of AI stage 2 are unchanged. Note that this figure shows the results with the addition of an extra impedance inverter at the input of the combined stages shown in Fig. 1. Hence the reciprocal impedance (or admittance) is converted back to an impedance with the addition of this extra impedance inverter. The addition of this inverter depends on the requirement of the amplifier and although it increases power consumption and die area it allows further tuning flexibility of the impedance function before being presented to the amplifier. Due to the isolation provided by the impedance inverters, the AI stages can be tuned independently of the other two stages. For example in Fig. 5 stages 1 and 3 are varied in frequency but this leaves stage 2 unaffected. It is noted that the impedance level of each band is within 5dB of each other. This has been achieved by tuning the g_m of the individual impedance inverter stages by varying the bias current at each stage. It was found that in order to maintain a near constant impedance level the g_m of each inverter stage needs to be set lower as the frequency of the associated AI stage increases.

The typical g_m used by each AI and the associated impedance inverter stage across the entire frequency band ranges from 0.07 to 0.3. Due to the low g_m values needed, each AI block consumes a total power of less than 5mW [5]. Hence the combined circuit has a low power dissipation. The values of capacitor C_1 range from 500fF down to 100fF. Capacitor C_2 ranges from 100fF to 500fF and C_3 ranges from 100fF to 1.4pF. As discussed above (discussion around Fig. 2)) the capacitor C_3 is a combination of on chip varactor, MOSFET switch and off chip BST tunable capacitor. The off chip capacitor is required to have a range from between 0.5pF to 2pF and is achievable in commercially available MEMS/BST components.

The zeros of the active impedance for example around 1.2GHz and 3.6GHz (see Fig. 5) translate into transmission zeros when the load is incorporated into an amplifier. This can be very useful for mitigating narrow band interference in high power interferer scenarios. There is however very limited control over these zeros due to their dependence on the values of C_1, C_3 and the g_m of the individual inverter stage attached to the AI. Aside from some flexibility in setting the values for C_1 and C_3 there is very little flexibility in setting all these three variables simultaneously. Hence there is a limited capability for freely positioning the impedance nulls. The position of the zeros can however be traded off for a degrade in the Q of that particular band as shown in Fig. 6. Varying capacitor C_2 allows the impedance nulls to be shifted at the expense of degrading Q factor of the associated resonant peak as shown in Fig. 6.

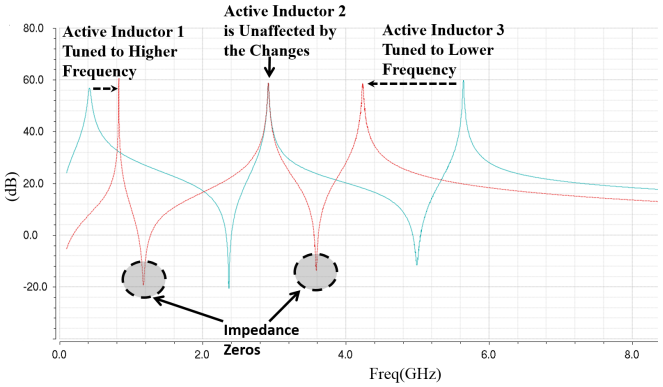

Fig. 5. Input impedance with different values of C_1, C_2, C_3 and the g_m of each impedance inverter stage. The y-axis shows impedance value in ohms converted to dB20 (20*Log10(Z_{ohms})).

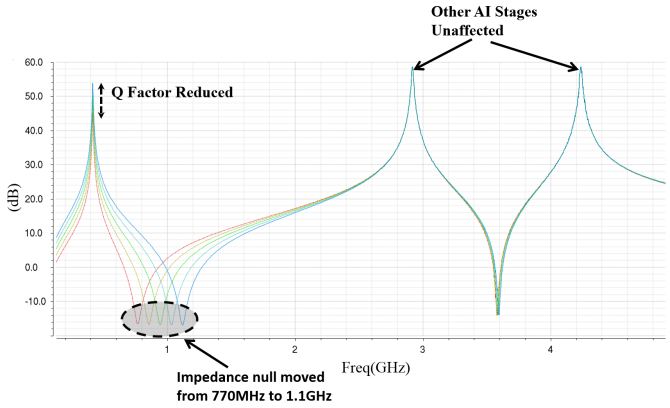

Fig. 6. Shows how variations in the Q factor can be traded off for controlling the position of the nulls in impedance. The y-axis shows impedance value in ohms converted to dB20 (20*Log10(Z_{ohms})).

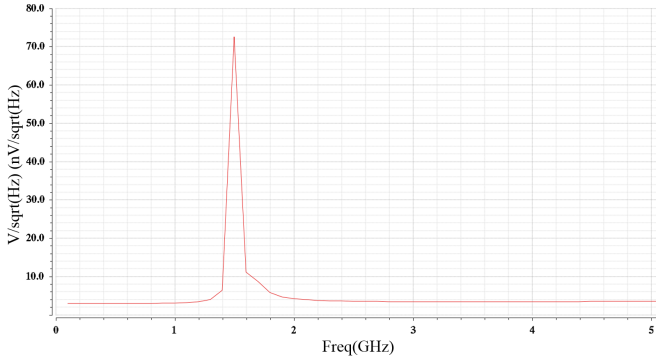

Fig. 7. Shows the average noise voltage at the output of the impedance inverter for centre frequency of 1.5GHz.

The major drawback of AI based circuits is that the noise of the AI block propagates through the rest of the circuit as discussed in [5] and [7]. The inclusion of impedance inverters has the advantage of reducing noise levels generated by the AI circuit. The noise voltage shown in Fig. 7 was taken at the output of the impedance inverter stage with its input connected to the AI block as shown in Fig. 1. This shows a value of 70nV/$\sqrt{Hz}$ and is an order of magnitude lower than the results for the AI circuit alone [7]. This shows the action of the impedance inverter in reducing noise levels generated by the AI block. Several techniques to overcome the noise problem in active inductor circuits have been developed [9]. Similar techniques are being investigated and it is expected these will be useful in further reducing the noise levels such that they will be suitable for front end low noise amplifier circuits.

This section has shown simulations of the pre-production circuit. This design is scheduled for fabrication in the next few months.

REFERENCES

[1] J. Borremans, G. Mandal, V. Giannini, B. Debaillie, M. Ingels, T. Sano, and B. Verbruggen, "A 40 nm CMOS 0.4–6 GHz receiver resilient to out-of-band blockers," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1659–1671, 2011.

[2] H. Hedayati, W.-F. A. Lau, N. Kim, V. Aparin, and K. Entesari, "A 1.8 dB NF blocker-filtering noise-canceling wideband receiver with shared TIA in 40 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 5, pp. 1148–1164, 2015.

[3] D. Murphy, H. Darabi, A. Abidi, A. A. Hafez, and M.-C. F. Chang, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, 2012.

[4] H. Hedayati, V. Aparin, and K. Entesari, "A+ 22dBm IIP3 and 3.5 dB NF wideband receiver with RF and baseband blocker filtering techniques," in *VLSI Circuits Digest of Technical Papers, 2014 Symposium on*. IEEE, 2014, pp. 1–2.

[5] C. Gamlath, E. Arabi, K. Morris, and M. Beach, "A 0.4-6GHz CMOS Tunable Load with Independent Q Tuning for 5G Filtering Applications," in *IET Conference Proceedings on Active and Passive RF Devices*. IET, 2017, pp. 5–6.

[6] S. Pipilos, Y. P. Tsividis, J. Fenk, and Y. Papananos, "A Si 1.8 GHz RLC filter with tunable center frequency and quality factor," *IEEE Journal of solid-state circuits*, vol. 31, no. 10, pp. 1517–1525, 1996.

[7] H. Xiao and R. Schaumann, "A 5.4-GHz high-Q tunable active-inductor bandpass filter in standard digital CMOS technology," *Analog integrated circuits and signal processing*, vol. 51, no. 1, pp. 1–9, 2007.

[8] H. Darabi, "A blocker filtering technique for SAW-less wireless receivers," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2766–2773, 2007.

[9] M. Moezzi and M. S. Bakhtiar, "Wideband LNA using active inductor with multiple feed-forward noise reduction paths," *IEEE transactions on microwave theory and techniques*, vol. 60, no. 4, pp. 1069–1078, 2012.

[10] J.-T. Yang, Y.-H. Lee, Y.-Y. Huang, Y.-M. Mu, and Y.-C. Ho, "A 0.18 um CMOS using high-Q active inductors for multi-band low noise amplifier," in *Electron Devices and Solid-State Circuits, 2007. EDSSC 2007. IEEE Conference on*. IEEE, 2007, pp. 1001–1004.

[11] Q. Li and Y. P. Zhang, "A 1.5-V 2–9.6-GHz inductorless low-noise amplifier in 0.13-μm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 10, pp. 2015–2023, 2007.

[12] J.-B. Yoon and C.-C. Nguyen, "A high-Q tunable micromechanical capacitor with movable dielectric for RF applications," in *Electron Devices Meeting, 2000. IEDM'00. Technical Digest. International*. IEEE, 2000, pp. 489–492.

[13] J. L. Hilbert, *Tunable RF Components and Circuits: Applications in Mobile Handsets*. CRC Press, 2015, vol. 51.

[14] X. Li, Z. Ni, L. Gu, Z. Wu, and C. Yang, "Micromachined high-performance RF passives in CMOS substrate," *Journal of Micromechanics and Microengineering*, vol. 26, no. 11, p. 113001, 2016.

[15] F. Seguin, B. Godara, F. Alicalapa, and A. Fabre, "2.2 GHz all-npn second-generation controlled conveyor in pseudoclass AB using 0.8-/spl mu/m BiCMOS technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, no. 7, pp. 369–373, 2004.